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PCEP Extension for Flexible Grid Networks
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Abstract

This document provides the Path Computation Element Communication Protocol (PCEP) extensions for the support of Routing and Spectrum Assignment (RSA) in Flexible Grid networks.

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1. Terminology

This document uses the terminology defined in [RFC4655], [RFC5440], and [RFC7698].

2. Requirements Language

The key words "MUST", "MUST NOT", "REQUIRED", "SHALL", "SHALL NOT", "SHOULD", "SHOULD NOT", "RECOMMENDED", "NOT RECOMMENDED", "MAY", and "OPTIONAL" in this document are to be interpreted as described in BCP 14 [RFC2119] [RFC8174] when, and only when, they appear in all capitals, as shown here.

3. Introduction

[RFC4655] defines a Path Computation Element (PCE)-based path computation architecture and explains how a Path Computation Element (PCE) may compute Label Switched Paths (LSP) in Multiprotocol Label Switching Traffic Engineering (MPLS-TE) and Generalized MPLS (GMPLS) networks at the request of Path Computation Clients (PCCs). A PCC is said to be any network component that makes such a request and may be, for instance, an Optical Switching Element within a Wavelength Division Multiplexing (WDM) network. The PCE, itself, can be located anywhere within the network, and may be within an optical switching element, a Network Management System (NMS) or Operational Support System (OSS), or may be an independent network server.

The PCE communications Protocol (PCEP) is the communication protocol used between a PCC and a PCE, and can also be used between cooperating PCEs. [RFC4657] sets out the common protocol requirements for PCEP. Additional application-specific requirements for PCEP are deferred to separate documents.

[RFC8780] provides the PCEP extensions for the support of Routing and Wavelength Assignment (RWA) in Wavelength Switched Optical Networks (WSON) based on the requirements specified in [RFC6163] and [RFC7449].

To allow efficient allocation of optical spectral bandwidth for systems that have high bit-rates, the International Telecommunication Union Telecommunication Standardization Sector (ITU-T) has extended its Recommendations [ITU-T_G.694.1] to include an enhanced Dense Wavelength Division Multiplexing (DWDM) grid by defining a set of nominal central frequencies, channel spacings, and the concept of the "frequency slot". In such an environment, a data-plane connection is switched based on allocated, variable-sized frequency ranges within the optical spectrum, creating what is known as a flexible grid (flexi-grid). [RFC7698] provides Framework and Requirements for GMPLS-Based Control of Flexi-Grid Dense Wavelength Division Multiplexing (DWDM) Networks.

The terms "Routing and Spectrum Assignment" (RSA) is introduced in [RFC7698] to refer to the process determines a route and frequency slot for an LSP. Hence, when a path is computed, the spectrum assignment process determines the central frequency and slot width. The term "Spectrum Switched Optical Networks" is also introduced in [RFC7698] to refer to a flexi-grid enabled DWDM network, which can be controlled by a GMPLS or PCE control plane.

This document provides PCEP extensions to support RSA in Flexi-grid networks.

Figure 1 shows one typical PCE-based implementation, which is referred to as the Combined Routing and Spectrum Assignment (RSA) [RFC7698]. With this architecture, the two processes of routing and spectrum assignment are accessed via a single PCE. This architecture is the base architecture from which the PCEP extensions are specified in this document.

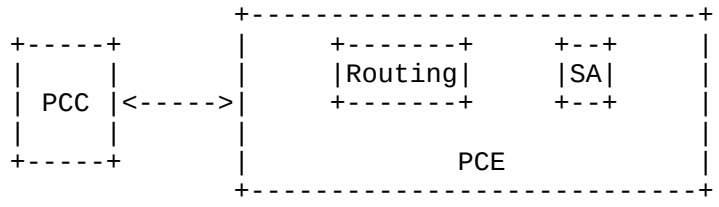


Figure 1: Combined Routing and Spectrum Assignment Architecture

4. Spectrum Assignment (SA) Object

This document aligns with GMPLS extensions for PCEP [RFC8779] for generic property such as label, label-set and label assignment noting that frequency is a type of label. Frequency restrictions and constraints are also formulated in terms of labels per [RFC7579].

Spectrum allocation can be performed by the PCE by different means:

a. By means of Explicit Label Control (ELC) where the PCE allocates which label to use for each interface/node along the path.

b. By means of a Label Set where the PCE provides a range of potential frequency slots to allocate by each node along the path.

Option b. allows distributed spectrum allocation (performed during signaling) to complete spectrum assignment. Additionally, given a range of potential spectrums to allocate, a PC Request SHOULD convey the heuristic / mechanism to the allocation.

The format Routing Backus-Naur Form (RBNF) [RFC5511] of a PCReq message per [RFC5440] after incorporating the Spectrum Assignment (SA) Object is as follows:

```
<PCReq Message> ::= <Common Header>
                        [<svec-list>]
                        <request-list>
   Where:
<request-list>::=<request>[<request-list>]
<request>::= <RP>
             <GENERALIZED ENDPOINTS>
                [<SA>]
                [other optional objects...]
```

If the SA Object is present in the PCReq message, it MUST be encoded after the GENERALIZED ENDPOINTS Object.

The SA Object-Class is TBD1 (to be assigned by IANA). The SA Object-Type is 1.

The format of the Spectrum Assignment (SA) Object body is as shown in Figure 2.

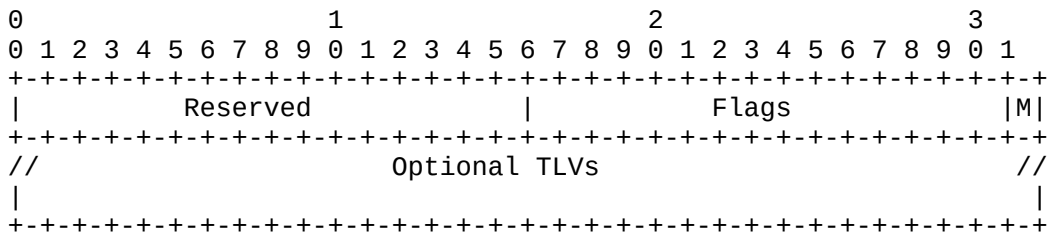


Figure 2: SA Object

Reserved (16 bits)

Flags (16 bits)

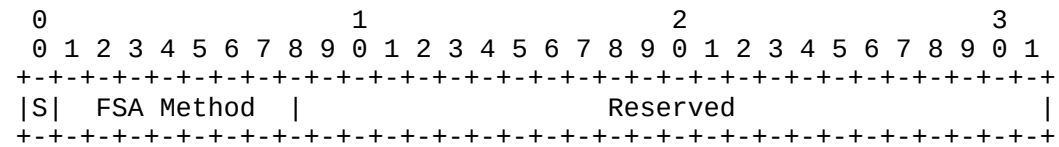
One Flag bit is allocated as follows:

M (Mode - 1 bit): M bit is used to indicate the mode of spectrum assignment. When the M bit is set to 1, this indicates that the spectrum assigned by the PCE must be explicit. That is, the selected way to convey the allocated spectrum is by means of Explicit Label Control (ELC) [RFC3472] for each hop of a computed LSP. Otherwise, when the M bit is set to 0, the spectrum assigned by the PCE needs not be explicit (i.e., it can be suggested in the form of Label Set Objects in the corresponding response, to allow distributed SA). In such case, the PCE MUST return a Label Set Field as described in Section 2.6 of [RFC7579] in the response. See Section 5 of this document for the encoding discussion of a Label Set Field in a PCRep message.

4.1. Frequency Slot Selection TLV

The Frequency Slot Selection TLV is used to indicate the frequency slot selection constraint in regard to the order of frequency slot assignment to be returned by the PCE. This TLV is only applied when the M bit is set in the SA Object specified in Section 4. This TLV SHOULD NOT be present and MUST be ignored when the M bit is set to 0.

The Frequency Slot Selection TLV value field is defined as:



Frequency Slot Assignment (FSA) Method (7 bits):

* 0: unspecified (any); This does not constrain the SA method used by a PCC This value is implied when the Frequency Slot Selection TLV is absent.

* 1: First-Fit. All the feasible frequency slots are numbered (based on ’n’ parameter), and this SA method chooses the available frequency slot with the lowest index, where ’n’ is the parameter in f = 193.1 THz + n x 0.00625 THz where 193.1THz is the ITU-T ’anchor frequency’ and ’n’ is a positive integer including 0 [RFC7698].

* 2: Random. This SA method chooses a feasible frequency slot value of ’n’ randomly.

* 3-127: Unassigned.

S (Symmetry, 1 bit): This flag is only meaningful when the request is for a bidirectional LSP (see [RFC5440]). 0 denotes requiring the same frequency slot in both directions; 1 denotes that different spectrums on both directions are allowed.

The Frequency Slot Selection TLV type is TBD2 (to be assigned by IANA).

If a PCE does not support the attribute(s), its behavior is specified below:

* S bit clear not supported: a PathErr MUST be generated with the Error Code "Routing Problem" (24) with error sub-code "Unsupported Frequency Slot Selection Symmetry value" (TBD3).

* FSA method not supported: a PathErr MUST be generated with the Error Code "Routing Problem" (24) with error sub-code "Unsupported Frequency Slot Assignment value" (TBD4).

4.2. Frequency Slot Restriction Constraint TLV

For any request that contains a frequency slot assignment, the requester (PCC) must be able to specify a restriction on the frequency slots to be used. This restriction is to be interpreted by the PCE as a constraint on the tuning ability of the origination laser transmitter or on any other maintenance related constraints.

The Frequency Slot Restriction Constraint TLV type is TBD5 (to be assigned by IANA). This TLV MAY appear more than once to be able to specify multiple restrictions. The TLV data is defined as shown in Figure 3.

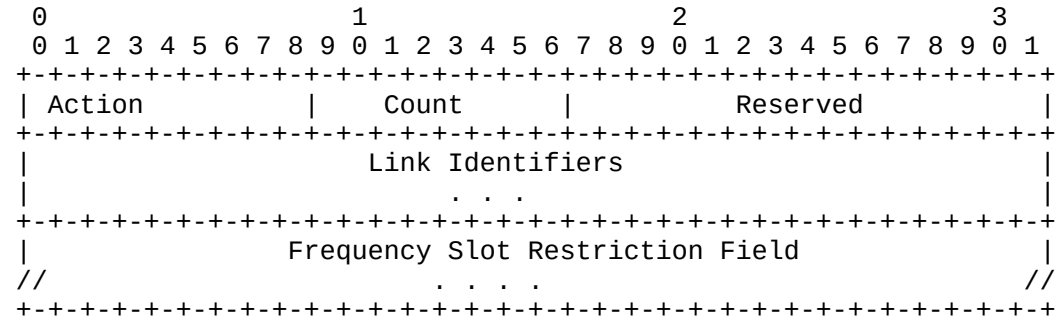


Figure 3: Spectrum Restriction Constraint TLV Encoding

The fields in the TLV are as follows:

* Action: 8 bits.

  - 0 - Inclusive List indicates that one or more link identifiers are included in the Link Set. Each identifies a separate link that is part of the set.

  - 1 - Inclusive Range indicates that the Link Set defines a range of links. It contains two link identifiers. The first identifier indicates the start of the range (inclusive). The second identifier indicates the end of the range (inclusive). All links with numeric values between the bounds are considered to be part of the set. A value of zero in either position indicates that there is no bound on the corresponding portion of the range. Note that the Action field can be set to 0 when unnumbered link identifier is used.

* Count: The number of the link identifiers (8 bits).

* Reserved: Reserved for future use (16 bits).

* Link Identifiers: Identifies each link ID for which restriction is applied. The length is dependent on the link format and the Count field. See Section 4.3.1 in [RFC8780] for Link Identifier encoding.

A PCC MAY add a frequency slot restriction that applies to all links by setting the Count field to zero and specifying just a set of frequency slots.

Note that all link identifiers in the same list must be of the same type.

4.2.1. Frequency Slot Restriction Field

The Frequency Slot Restriction Field of the Frequency slot restriction TLV is encoded as defined in Section 4.2 of [RFC8363].

5. Encoding of an RSA Path Reply

This section provides the encoding of an RSA Path Reply, in the PCRep/PCUpd message, for frequency slot allocation as discussed in Section 4. The Spectrum Allocation TLV type is TBD6 (to be assigned by IANA). The TLV data is defined as shown in Figure 4.

[RFC7570] describes how an attribute TLV ([RFC5420]) can be carried in an ERO as a TLV within an LSP Attribute Subobject to provide a per-hop description of an LSP attribute. The Spectrum Assignment TLV can be carried in the LSP Attribute Subobject to indicate the spectrum to be assigned on the identified link.

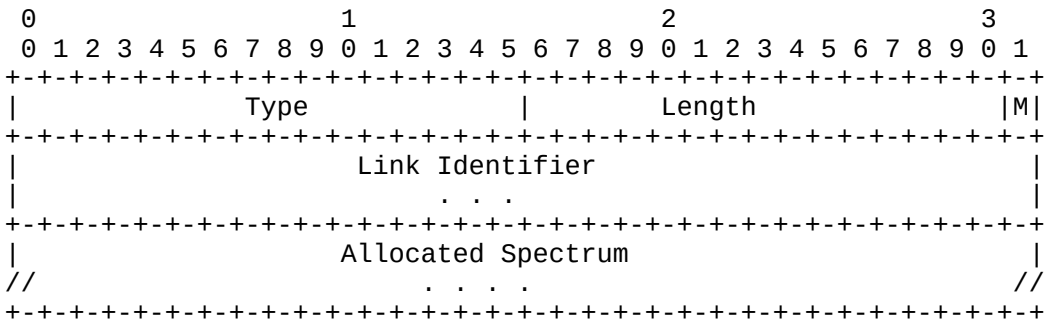


Figure 4: Spectrum Allocation TLV Encoding

* Type (16 bits): The type of the TLV (TBD6).

* Length (15 bits): The length of the TLV including the Type and Length fields.

* M (Mode): 1 bit

- 1 indicates the allocation is under Explicit Label Control.

- 0 indicates the allocation is expressed in Label Sets.

* Link Identifiers: Identifies each link ID for which restriction is applied. The length is dependent on the link format and the Count field. See Section 4.3.1 in [RFC8780] for Link Identifier encoding.

* Allocated Spectrum (variable): Indicates the spectrum allocated to the link identifier. See Section 4.3 of [RFC7699] for encoding details.

Note that all link identifiers in the same list must be of the same type.

5.1. Error Indicator

To indicate errors associated with the RSA request, a new Error Type and subsequent error-values are defined as follows for inclusion in the PCEP-ERROR Object:

A new Error-Type (TBD7) and subsequent error-values are defined as follows:

* Error-Type=TBD7; Error-value=1: if a PCE receives an RSA request and the PCE is not capable of processing the request due to insufficient memory, the PCE MUST send a PCErr message with a PCEP-ERROR Object (Error-Type=TBD7) and an Error-value(Error-value=1). The PCE stops processing the request. The corresponding RSA request MUST be cancelled at the PCC.

* Error-Type=TBD7; Error-value=2: if a PCE receives an RSA request and the PCE is not capable of RSA computation, the PCE MUST send a PCErr message with a PCEP-ERROR Object (Error-Type=TBD7) and an Error-value (Error-value=2). The PCE stops processing the request. The corresponding RSA computation MUST be cancelled at the PCC.

5.2. NO-PATH Indicator

To communicate the reasons for not being able to find RSA for the path request, the NO-PATH Object can be used in the corresponding response. The format of the NO-PATH Object body is defined in [RFC5440]. The object may contain a NO-PATH-VECTOR TLV to provide additional information about why a path computation has failed.

One new bit flag is defined to be carried in the Flags field in the NO-PATH-VECTOR TLV carried in the NO-PATH Object.

* Bit TBD8: When set, the PCE indicates no feasible route was found that meets all the constraints (e.g., spectrum restriction, etc.) associated with RSA.

6. Manageability Considerations

Manageability of flexi-grid Routing and Spectrum Assignment (RSA) with PCE must address the following considerations:

6.1. Control of Function and Policy

In addition to the parameters already listed in Section 8.1 of [RFC5440], a PCEP implementation SHOULD allow configuring the following PCEP session parameters on a PCC:

* The ability to send a Flexi-Grid RSA request.

In addition to the parameters already listed in Section 8.1 of [RFC5440], a PCEP implementation SHOULD allow configuring the following PCEP session parameters on a PCE:

* The support for Flexi-Grid RSA.

* A set of Flexi-Grid RSA specific policies (authorized sender, request rate limiter, etc).

These parameters may be configured as default parameters for any PCEP session the PCEP speaker participates in, or may apply to a specific session with a given PCEP peer or a specific group of sessions with a specific group of PCEP peers.

6.2. Information and Data Models

Extensions to the PCEP YANG module may include to cover the Flexi-Grid RSA information introduced in this document. Liveness Detection and Monitoring Mechanisms defined in this document do not imply any new liveness detection and monitoring requirements in addition to those already listed in Section 8.3 of [RFC5440].

6.3. Verifying Correct Operation

Mechanisms defined in this document do not imply any new verification requirements in addition to those already listed in section 8.4 of [RFC5440].

6.4. Requirements on Other Protocols and Functional Components

The PCE Discovery mechanisms ([RFC5088] and [RFC5089]) may be used to advertise Flexi-Grid RSA path computation capabilities to PCCs.

6.5. Impact on Network Operation

Mechanisms defined in this document do not imply any new network operation requirements in addition to those already listed in Section 8.6 of [RFC5440].

7. Implementation Status

[NOTE TO RFC EDITOR: This whole section and the reference to [RFC7942] is to be removed before publication as an RFC]

This section records the status of known implementations of the protocol defined by this specification at the time of posting of this Internet-Draft, and is based on a proposal described in [RFC7942].

The description of implementations in this section is intended to assist the IETF in its decision processes in progressing drafts to RFCs. Please note that the listing of any individual implementation here does not imply endorsement by the IETF. Furthermore, no effort has been spent to verify the information presented here that was supplied by IETF contributors. This is not intended as, and must not be construed to be, a catalog of available implementations or their features. Readers are advised to note that other implementations may exist.

According to [RFC7942]], "this will allow reviewers and working groups to assign due consideration to documents that have the benefit of running code, which may serve as evidence of valuable experimentation and feedback that have made the implemented protocols more mature. It is up to the individual working groups to use this information as they see fit".

7.1. Huawei Technologies

At the time of posting the -10 version of this document, Huawei has implemented some of the features specified in this document, on the WDM network. Details are as follow:

Organization: Huawei Technologies Co.,Ltd.
Implementation: Huawei's WDM systems
Description: supporting PCE Protocol with WDM extensions
Maturity Level: supported features
Coverage: Partial
Contact: zhenghaomian@huawei.com

8. Security Considerations

This document has no requirement for a change to the security models within PCEP. However, the additional information distributed in order to address the RSA problem represents a disclosure of network capabilities that an operator may wish to keep private. Consideration should be given to securing this information.

9. IANA Considerations

This document requests IANA actions to allocate code points for the objects and sub-registries defined in this document.

9.1. New PCEP Object

As described in Section 4, a new PCEP Object is defined to carry frequency slot assignment-related constraints. IANA is requested to allocate the following from 'PCEP Objects' sub-registry (http://www.iana.org/assignments/pcep/pcep.xhtml#pcep-objects):

Object Class Value	Name	Object Type	Reference
TBD1	SA	1: Spectrum Assignment	[This.I-D]

9.2. New PCEP TLV: Frequency Slot Selection TLV

As described in Section 4.1, a new PCEP TLV is defined to indicate spectrum selection constraints. IANA is requested to allocate this new TLV from the 'PCEP TLV Type Indicators' subregistry (http://www.iana.org/assignments/pcep/pcep.xhtml#pcep-tlv-type-indicators).

Value	Description	Reference
TBD2	Spectrum Selection	[This.I-D]

9.3. New PCEP TLV: Frequency Slot Restriction Constraint TLV

As described in Section 4.2, a new PCEP TLV is defined to indicate wavelength restriction constraints. IANA is requested to allocate this new TLV from the 'PCEP TLV Type Indicators' subregistry (http://www.iana.org/assignments/pcep/pcep.xhtml#pcep-tlv-type-indicators).

Value	Description	Reference
TBD5	Frequency Slot Restriction Constraint	[This.I-D]

9.4. New PCEP TLV: Spectrum Allocation TLV

As described in Section 5, a new PCEP TLV is defined to indicate the allocation of frequency slots(s) by the PCE in response to a request by the PCC. IANA is requested to allocate this new TLV from the "PCEP TLV Type Indicators" subregistry (http://www.iana.org/assignments/pcep/pcep.xhtml#pcep-tlv-type-indicators).

Value	Description	Reference
TBD6	Spectrum Allocation	[This.I-D]

9.5. New No-Path Reasons

As described in Section 5.2, a new bit flag are defined to be carried in the Flags field in the NO-PATH-VECTOR TLV carried in the NO-PATH Object. This flag, when set, indicates that no feasible path was found that meets all the RSA constraints (e.g., spectrum restriction, signal compatibility, etc.) associated with an RSA path computation request.

IANA is requested to allocate this new bit flag from the "PCEP NO-PATH-VECTOR TLV Flag Field" subregistry (http://www.iana.org/assignments/pcep/pcep.xhtml#no-path-vector-tlv).

Bit	Description	Reference
TBD8	No RSA constraints met	[This.I-D]

9.6. New Error-Types and Error-Values

As described in Section 5.1, new PCEP error codes are defined for WSON RWA errors. IANA is requested to allocate from the 'PCEP-ERROR Object Error Types and Values' sub-registry (http://www.iana.org/assignments/pcep/pcep.xhtml#pcep-error-object)

Error-Type	Meaning	Error-Value	Reference
TBD7	Flexi-Grid RSA Error	1: Insufficient Memory	[This.I-D]
		2: RSA computation Not supported	[This.I-D]

9.7. New Error-Values for Existing Error Type (24)

As discussed in Section 4.1, IANA is requested to allocate two new PathErr values for the Existing Error Type (24):

Meaning	Error-Value	Reference
Unsupported Frequency Slot Selection Symmetry value	TBD3	[This.I-D]
Unsupported Frequency Slot Assignment value	TBD4	[This.I-D]

10. Acknowledgements

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