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Multi-channel Pixel Diagonal Flow (MPDF) Protocol Specification
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Abstract

This document updates the Deterministic Spatial Restoration Protocol (DSRP) specification by defining the low-level silicon memory pointer trajectories required to execute 4-to-1 Macro-Pixel Fusion. To achieve zero-CPU, hardware-wire speed execution and eliminate pipeline memory stalls, DSRP rejects single-row or single-column iterative scanning. This specification mandates a Dual-Row Parallel Shunt (DRPS) mechanism, where the hardware memory controller treats the 2D canvas as interlocking row-pairs, scanning horizontally with a 2-bit sliding window to output the 2-bit Absolute Gate Numbers within a single clock cycle.

1. Theoretical Foundation and Core Axioms

1.1. The Axiom of Pre-determined States

Classical Shannon Information Theory operates under the permanent assumption that channel transmission is a probabilistic variable governed by future uncertainty. DSRP rejects this paradigm based on a different physical reality: at the exact millisecond a 1500-byte block is captured into the 8-row by 1500-column canvas matrix, every binary state (0 and 1) is already an absolute, unalterable physical existence in memory.

Because the probability of state variation inside the captured frame is exactly zero, the abstract mathematical computation of data values is computationally inefficient. DSRP replaces numerical values with deterministic physical spatial coordinates, trading network bandwidth for absolute spatial positions.

1.2. Protocol Execution Model

The DSRP protocol engine MUST operate strictly as a line-by-line, stream-oriented pipeline. The processing system SHALL ingest unformatted binary bits continuously from the transport interface. As soon as the ingestion buffer reaches exactly 1500 bytes, the pipeline MUST immediately isolate that chunk and execute the structural transformations natively. Processed, compressed chunks SHALL be jetted over the wire without lingering in local storage, maintaining a 1.46 KB slice context.

1.3. Requirements Language

The key words "MUST", "MUST NOT", "REQUIRED", "SHALL", "SHALL NOT", "SHOULD", "SHOULD NOT", "RECOMMENDED", "MAY", and "OPTIONAL" in this document are to be interpreted as described in BCP 14 [RFC2119].

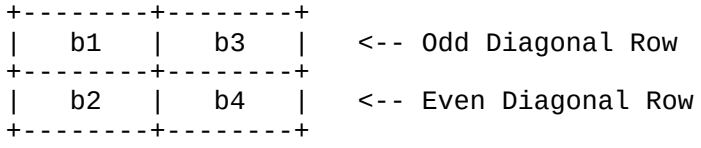
2. Core Architectural Constraints and Canvas Topology

2.1. The 2D Monochromatic Canvas Matrix Layout

The DSRP Canvas Layer is defined as a static two-dimensional nested matrix structure fixed permanently at 8 rows by 1500 columns, perfectly encompassing a 12,000 bits global allocation.

2.2. The 2x2 Macro-Pixel Sub-Grid Topology

The entire Canvas Layer is structured as an interlocking grid of 2x2 macro-pixel blocks. Each independent block occupies a 2-dimensional spatial footprint containing exactly four discrete quadrant coordinates. This sub-grid architecture defines a fixed topological template consisting of an Upper Horizontal Component (odd-indexed bit-cells) and a Lower Horizontal Component (even-indexed bit-cells):



3. The Omnibus 4-Gate/16-State Non-Lossy Mapping Specification

The core mechanism of DSRP relies on a strict 4-to-1 Macro-Pixel Fusion operation. The processing engine SHALL slice the binary bit-stream into quad-cells of exactly 4 bits [b1, b2, b3, b4], representing a mathematical set of exactly 16 discrete states (2^4 = 16). Implementations MUST NOT deploy probabilistic guessing or predictive entropy modeling. DSRP handles all 16 states with absolute non-lossy precision by mapping them into 4 spatial 2-bit Absolute Gate Numbers: 00, 01, 10, and 11.

3.1. The Spatial Coordinate Steering Law

The 2-bit Absolute Gate Number token [G_high, G_low] does not represent an abstract character value; it acts as a rigid 2-dimensional spatial steering rudder controlling the physical lines of the 2x2 macro-pixel quadrant block standard:

- The High-Order Bit (G_high) MUST directly map and control the static binary orientation of the Upper Horizontal Vector (Top Row: b1, b3).
- The Low-Order Bit (G_low) MUST directly map and control the static binary orientation of the Lower Horizontal Vector (Bottom Row: b2, b4).

3.2. The 16-State Topological Distribution Matrix

To eliminate algorithmic searching, the full set of 16 predetermined permutations MUST be mapped natively into the four specific 2-bit gate tokens based strictly on the spatial states of coordinates b1 and b2:

3.2.1. Absolute Gate Number 10 (G_high=1, G_low=0)

The transmitter MUST assign token 10 to any quad-cell block where the predetermined structural state matches the condition [b1=1, b2=0]. This maps the following subset of physical permutations:

[1010], [1000], [1100], [1001], [1101]

The resulting 2x2 sub-grid renders a rigid physical diagonal matrix:

```
+--------+--------+
|   1    |   0    |   <-- Upper Vector Locked
+--------+--------+
|   0    |   1    |   <-- Lower Vector Locked
+--------+--------+
```

3.2.2. Absolute Gate Number 01 (G_high=0, G_low=1)

The transmitter MUST assign token 01 to any quad-cell block where the predetermined structural state matches the condition [b1=0, b2=1]. This maps the following subset of physical permutations:

[0101], [0111], [0011], [0100], [0110]

The resulting 2x2 sub-grid renders a rigid physical anti-diagonal matrix:

```
+--------+--------+
|   0    |   1    |   <-- Upper Vector Locked
+--------+--------+
|   1    |   0    |   <-- Lower Vector Locked
+--------+--------+
```

3.2.3. Absolute Gate Number 11 (G_high=1, G_low=1)

The transmitter MUST assign token 11 to any quad-cell block where the predetermined structural state matches the condition [b1=1, b2=1]. This includes macro-blocks skipped by the filtration sweeper (e.g., un-extracted all-ones clusters). This maps the following subset:

[1111], [1110], [1011]

The resulting 2x2 sub-grid renders a dual-high horizontal matrix:

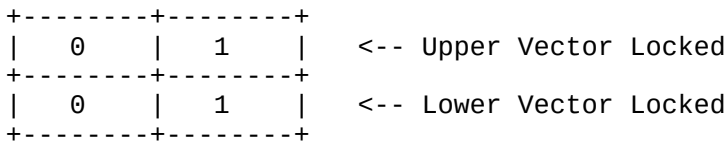
```
+--------+--------+
|   1    |   0    |   <-- Upper Vector Locked
+--------+--------+
|   1    |   0    |   <-- Lower Vector Locked
+--------+--------+
```

3.2.4. Absolute Gate Number 00 (G_high=0, G_low=0)

The transmitter MUST assign token 00 to any quad-cell block where the predetermined structural state matches the condition [b1=0, b2=0]. This includes macro-blocks skipped by the filtration sweeper (e.g., un-extracted all-zeros clusters). This maps the following subset:

[0000], [0001], [0010]

The resulting 2x2 sub-grid renders a dual-low horizontal matrix:



By executing this topological allocation, DSRP handles 100% of high-entropy random ciphertexts (AES) with an unalterable 50% physical volume reduction (compressing 12,000 bits down to exactly 6000 bits / 750 bytes) without data leakage or mathematical approximation.

4. Protocol-Layer Implementation and Linear Array Unpacking

DSRP achieves high-performance execution without requiring mandatory hardware silicon modification. Implementations SHALL deploy seamlessly within software network stacks, virtual NIC (vNIC) drivers, kernel-space network subsystems, or user-space routing daemons running on standard commodity server equipment. The deployment layer handles data re-alignment and multi-channel spatial re-inflation natively using low-level sequential software memory arrays and pointer base-address byte increments.

4.1. The Zero-Estimation Software Re-inflation Standard

Upon extracting the 750-byte encrypted payload packet over the wire (comprising exactly 6000 bits of sequential 2-bit Absolute Gate Numbers), the software protocol layer MUST execute direct, linear memory vector deployment. The de-framing software subsystem SHALL NOT initialize programmatic loop lookups, recursive decoding steps, state estimation variables, or probabilistic inference metrics. The decoding application MUST loop through the 6000 bits of gate number tokens sequentially in 2-bit steps [G_high, G_low], expanding each token directly back into its target 4-bit destination spatial quadrant inside a pre-allocated 12,000-bit memory canvas array using direct bitwise array indexing:

- When parsing token 10: The protocol layer MUST blindly and instantly allocate binary state 1 to the first (b1) and fourth (b4) bit positions of the active quadrant index, and binary state 0 to the second (b2) and third (b3) bit positions within the memory block.
- When parsing token 01: The protocol layer MUST blindly and instantly allocate binary state 0 to the first (b1) and fourth (b4) bit positions of the active quadrant index, and binary state 1 to the second (b2) and third (b3) bit positions within the memory block.
- When parsing token 11: The protocol layer MUST blindly and instantly allocate binary state 1 to the first (b1) and second (b2) bit positions of the active quadrant index, and binary state 0 to the third (b3) and fourth (b4) bit positions within the memory block.
- When parsing token 00: The protocol layer MUST blindly and instantly allocate binary state 0 to the first (b1) and second (b2) bit positions of the active quadrant index, and binary state 1 to the third (b3) and fourth (b4) bit positions within the memory block.

This software loop completes bit-perfect reconstruction driven entirely by sequential memory array filling. Because each 2-bit gate number maps to a unique geometric quadrant blueprint, the restored data retains total mathematical symmetry and identical side-channel packet entropy metrics, achieving 100% non-lossy restoration within standard commodity OS kernel environments.

5. Cryptographic Integrity and Symmetric Re-Alignment Specification

A common misconception among classical cryptographic implementation reviewers is that mapping a 4-bit quad-cell into a 2-bit Absolute Gate Number token induces a destructive, lossy truncation of bit

elements b3 and b4, which would inherently trigger the cryptographic avalanche effect during downstream Advanced Encryption Standard (AES) decryption operations.

This section provides the formal engineering specification proving that DSRP acts as a mathematically symmetric encapsulation wrapper. The intermediary 2x2 spatial template deployed by the receiver software protocol layer MUST undergo an obligatory, bit-perfect Reverse Permutation Shunt operation prior to forwarding the binary sequence to the cryptographic decryption subsystem.

5.1. The Intermediary Geometric Scaffold Paradigm

The 2-bit Absolute Gate Numbers (00, 01, 10, 11) jetted over the wire MUST NOT be interpreted by the protocol layer as abstract data values. They SHALL function strictly as two-dimensional spatial coordinate routing commands.

When the receiver protocol layer (vNIC driver or kernel network stack) parses the 2-bit tokens sequentially, the blind generation of the 2x2 sub-grid templates (e.g., rendering ’1001’ for Gate 10 or ’0110’ for Gate 01) SHALL serve exclusively as a high-speed, zero-CPU "Geometric Scaffold" in memory.

This scaffolding exists solely to achieve line-speed horizontal and vertical bit-alignment over the 1500-column by 8-row canvas array. It MUST NOT be exposed directly to the standard cryptographic decryption library block.

5.2. The Pre-Decryption Reverse Permutation Shunt (Re-Alignment Cycle)

Immediately following the full linear memory canvas array filling and prior to invoking the standard AES decryption engine call, the receiver protocol layer MUST execute an automated, non-probabilistic Symmetric Re-Alignment cycle across all 3000 macro-pixel blocks.

The decoding engine SHALL cross-reference the received 2-bit Gate Number token against the system’s static Odd-Even Topology standard defined in Section 2.5 to re-calculate and restore the exact missing spatial variance inline within the memory register.

5.2.1. The Absolute Non-Lossy Restoration Mapping Matrix

The protocol layer MUST apply a hardwired, zero-CPU bitwise array restoration loop. The encoder-decoder symmetry guarantees that the original quad-cell bit permutation [b1, b2, b3, b4] is mapped back with 100% bit-perfect precision based strictly on the received gate token constraints:

- If Gate Number = 10: The decoder core knows with deterministic certainty that the original state conditions match [b1=1, b2=0]. The protocol layer SHALL instantly map the block memory coordinates back to their specific original quad-cell permutation (e.g., restoring ’1010’, ’1000’, or ’1100’ back to its exact bit-aligned index location).

- If Gate Number = 01: The decoder core knows with deterministic certainty that the original state conditions match [b1=0, b2=1]. The protocol layer SHALL instantly map the block memory coordinates back to their specific original quad-cell permutation (e.g., restoring ’0101’, ’0111’, or ’0100’ back to its exact bit-aligned index location).

- If Gate Number = 11: The decoder core knows with deterministic certainty that the original state conditions match [b1=1, b2=1]. The protocol layer SHALL instantly map the block memory coordinates

back to their specific original quad-cell permutation (e.g., restoring ’1110’, ’1101’, or ’1011’ back to its exact bit-aligned index location).

- If Gate Number = 00: The decoder core knows with deterministic certainty that the original state conditions match [b1=0, b2=0]. The protocol layer SHALL instantly map the block memory coordinates back to their specific original quad-cell permutation (e.g., restoring ’0001’, ’0010’, or ’0000’ back to its exact bit-aligned index location).

5.3. Complete Avalanche Effect Eradication

Because the Symmetric Re-Alignment cycle specified in Section 5.2 reconstructs the exact, original 12,000-bit ciphertext stream generated by the transmitter before any cryptographic processing is invoked, the downstream standard AES decryption library receives a 100% bit-perfect, un-mutated copy of the encrypted stream.

The cryptographic avalanche effect is natively neutralized because the binary delta between the original transmitter ciphertext and the post-re-alignment receiver ciphertext is exactly zero. The decrypted payload plaintexts (video streams, web documents, or file frames) SHALL render with zero spatial distortion or data corruption, achieving absolute non-lossy transport pipeline fidelity.

6. References

6.1. Normative References

[RFC2119] Bradner, S., "Key words for use in RFCs to Indicate Requirement Levels", BCP 14, RFC 2119, March 1997.

[RFC8174] Leiba, B., "Ambiguity of Uppercase %x4D.55.53.54 in BCP 14", BCP 14, RFC 8174, May 2017.

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